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| 10/815,966 | 03/31/2004 | Scott R. Sahaida | 884.C31US1 | 7702 |

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| EXAMINER | |
|---|---|
| SMOOT, STEPHEN W | |

| ART UNIT | PAPER NUMBER |
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| 2813 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

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| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/815,966 | SAHAIDA ET AL. | |
| | Examiner | Art Unit | |
| | Stephen W. Smoot | 2813 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-11 and 22-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-11,22,25 and 26* is/are rejected.

7)☒ Claim(s) *4,5,23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20070718*.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

This Office action is in response to applicant's reply filed on 18 September 2006.

### *Response to Arguments*

1. Applicant's arguments, see pages 5-12, filed 18 September 2006, with respect to the prior art rejections of claims 1-11, 22-26 under 35 USC 102 or 35 USC 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, new grounds of rejection are made in view of Mess et al. (US 2002/0195697 A1).

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 7-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Mess et al. (US 2002/0195697 A1).

Referring to Figs. 28-29 and paragraph [0082], Mess et al. disclose a method for stacking plural rectangular-shaped semiconductor die (60) on a substrate (70) with the alternating die (60C, 60D in Fig. 29) offset so that bond pads (54C) located on two opposing sides of a die (60C) are exposed for wire bonding with bond wires (62C) to the substrate (70) while the two remaining opposing sides are covered by the overlying die (60D). Also, two semiconductor die (60A, 60B) underlie die (60C) as shown in Fig. 28. Mess et al. further disclose that silicon spacers with the same shape can be inserted between semiconductor die in the stack (also see paragraph [0054]) and that the stack may include additional die besides the four die that are described (also see paragraph [0084]). These are all of the limitations set forth in claims 1, 7-9, 11 of the applicant's invention.

Regarding claim 2, the die can include flash memory (also see paragraphs [0057] and [0083]).

Regarding claims 3, 10, adhesive (78 in Fig. 13) is used above and below the die (60A) for bonding the die (60A) to the substrate (70) and to the next overlying die (60B) (also see paragraphs [0058] and [0068]).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mess et al. (US 2002/0195697 A1) as applied to claim 1 above, and further in view of Pai et al (US 2002/0140073 A1).

As shown above, Mess et al. anticipate claim 1 of the applicant's invention. However, Mess et al. do not expressly teach or suggest that the spacer is about 1 mm away from the third and fourth sides, which is the further limitation to claim 1 as set forth in claim 6 of the applicant's invention. Pai et al. suggest that a spacer (160) can be separated at least 6 mils (i.e. 0.15 mm) from bonding pads (110a) (see Fig. 2 and paragraph [0018]).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to separate the spacer of Mess et al. about 1 mm away from the two opposing sides with corresponding bond pads of the underlying die through routine experimentation, since it has been held that the discovery of optimum values of result effective variables in known processes is ordinarily within the skill level of the art unless

the applicant can show unexpected results for this parameter [see *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980)].

6. Claims 22, 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mess et al. (US 2002/0195697 A1) in view of He et al. (US 2004/0039859 A1).

Referring to Figs. 28-29 and paragraph [0082], Mess et al. disclose a method for stacking plural rectangular-shaped semiconductor die (60) on a substrate (70) with the alternating die (60C, 60D in Fig. 29) offset so that bond pads (54C) located on two opposing sides of a die (60C) are exposed for wire bonding with bond wires (62C) to the substrate (70) while the two remaining opposing sides are covered by the overlying die (60D). Also, two semiconductor die (60A, 60B) underlie die (60C) as shown in Fig. 28. Mess et al. further disclose that silicon spacers with the same shape can be inserted between semiconductor die in the stack (also see paragraph [0054]). Further, Mess et al. disclose that the die can include flash memory (also see paragraphs [0057] and [0083]). These are limitations as set forth in claims 22, 26 of the applicant's invention.

However, Mess et al. lack the claim features of a buss and a memory coupled to the buss, which are limitations of claim 22.

Referring to Fig. 3 and paragraphs [0023] to [0026], He et al. teach an electronic system (40) that includes a system bus (42) for coupling various components like memory (50) in the form of random access memory (52).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Mess et al. and He et al. in

order to use the flash memory of Mess et al. as the random access memory of He et al., because He et al. recognize that memory can be coupled to a system bus (see Fig. 3 and paragraphs [0023] to [0026]).

7. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mess et al. (US 2002/0195697 A1) and He et al. (US 2004/0039859 A1) as applied to claim 22 above, and further in view of Li et al. (US 6,493,861 B1).

As shown above, the combination of Mess et al. and He et al. has all of the limitations of claim 22. However, this combination does not expressly teach or suggest a voltage source electrically coupled to the semiconducting device, which is the further limitation to claim 22 as set forth in claim 25 of the applicant's invention. Li et al. teach that a bus can be used to couple a microprocessor to memory and to a power supply (see column 13, line 36 to column 14, line 67).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Mess et al., He et al., and Li et al. in order to include the microprocessor and power supply coupled to the bus as taught by Li et al. Li et al. recognize that the microprocessor can be utilized to communicate power supply signals to the memory (see column 14, lines 51-60).

## *Allowable Subject Matter*

8. Claims 4-5, 23-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: Claims 4-5, 23-24 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, a semiconductor device that includes a spacer covering active circuitry on an upper surface of a die, wherein the spacer extends from a first side of the die to an opposing second side of the die and extends near a third side of the die and an opposing fourth side of the die so that active circuitry is exposed near the third and fourth sides, and wherein the spacer also includes at least one section that extends to the third side of the die.

## *Conclusion*

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wang et al., Goller et al., and Lee et al. teach stacked chip package assemblies that utilize spacers.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on Monday to Friday from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

sws

Stephen W. Smoot

STEPHEN W. SMOOT
PRIMARY EXAMINER